REMARKS

This is in response to the Office Action of 13 April 2004. Claims 1-2 are pending in the application, and Claims 1-2 have been rejected.

By this Response and Amendment, Claims 1-2 have been amended in a non-narrowing manner, new Claims 3-11 have been added, a Replacement Sheet is provided with text labels added to the figure, and arguments are presented traversing a portion of the objections to the drawings, and traversing the rejection of Claims 1-2.

No new matter has been added.

In view of the amendments above and remarks below, Applicants respectfully request reconsideration and further examination.

About The Invention

The present invention relates generally to combining a synchronous digital circuit with an asynchronous digital circuit such that the synchronous circuit provides and holds data at an input of the asynchronous circuit while the asynchronous circuit computes a digital result based on the data provided.

Objection to the Drawings

The drawings have been objected to under 37 CFR 1.83(a). More particularly, the Examiner states that the time duration of the converting operation in comparison with the time interval to the next change of data present at the output must be shown or cancelled from the claims. Additionally, the Examiner states that text labels must be associated with the numbers indicating boxes or signals to fully illustrate the claimed invention. The Examiner has required a proposed drawing correction or corrected drawings.

With respect to the Examiner's requirement for text labels, submitted herewith is a Replacement Sheet in which text labels as required by the

Examiner have been added.

With respect to the Examiner's requirement to show the time duration of the converting operation in comparison with the time interval to the next change of data present at the output, Applicants respectfully traverse this requirement and request that it be withdrawn.

The figure as filed illustrates the elements of the claimed invention, i.e., a data-processing unit and a converting unit; and further illustrates communication paths between the data-processing unit and the converting unit. Applicants respectfully submit that the specification makes clear that the converting unit is an asynchronous logic block having a data path through which data propagates more quickly than the input data presented to it changes. In other words the input data hold time is greater than the conversion unit processing time.

Applicants respectfully submit that just as there is no requirement to show additional details in the block diagram figure illustrating encryption, compression, or error correction functions of the converting unit, (all of which are present in the Claims), there should be no requirement to show comparative operational times in this structural block diagram. Applicants further assert that all those skilled in the field of electrical engineering would comprehend Applicants' invention as illustrated.

In view of the foregoing, Applicants request that the requirement to amend the drawing to show the time duration of the converting operation in comparison with the time interval to the next change of data present at the output, be withdrawn.

Non-Narrowing Amendment of Claims 1 and 2

Independent Claim 1 has been amended in a non-narrowing manner to delete the reference numerals therein.

Dependent Claim 2 has also been amended in a non-narrowing manner. Firstly, the preamble has been amended so that it begins with the word "The"

rather than with the word "A". Secondly, the language "preferably a CRC operation" has been deleted.

Rejections under 35 USC 103(a)

Claims 1-2 have been rejected under 35 USC 103(a) as being unpatentable over Rowan, et al., (US Patent 5,140,248) in view of Ryan (US Patent 6,359,946).

Applicants respectfully traverse the rejection of Claims 1-2 under 35 USC 103(a) and request that the rejection be withdrawn.

Ryan teaches synchronization logic for synchronizing a sample clock to an asynchronous data sample. This is completely different from Applicants' claimed invention. The invention, defined by Claims 1-2, team an asynchronous digital co-processor (i.e., converting unit) with a synchronous digital data processing unit. More particularly, the synchronous unit provides and holds data at an input of the asynchronous unit until the asynchronous computation (i.e., conversion) has been completed. No synchronization logic is used.

The Examiner's citation of Ryan is directed to synchronizing two units, which is simply not done in the claimed invention. The combination of references does not appear to disclose, suggest, or motivate the invention defined by the Claims.

For at least the reasons set forth above, Applicants respectfully request that the rejection of Claims 1-2 be withdrawn.

New Claims 3-11

New Claim 3, which depends from amended Claim 1, recites that the converting operation is a CRC operation. Support for new Claim 3 can be found in the specification at pages 3-4.

New Claims 4-5, which depend from amended Claim 1, are directed to the

data pathway connections of present invention. Support for new Claims 4-5 can be found at pages 4, lines 3-6; and in the figure.

New Claims 6-9 are directed to a digital system that includes both a synchronous digital circuit and an asynchronous digital circuit, coupled to each other, wherein the synchronous circuit provides data to the asynchronous circuit, and the asynchronous circuit computes a digital result faster than the synchronous circuit can provide new data to the asynchronous circuit. Support for these Claims can be found in the specification from page 2, line 10, through page 4, line 9, and in the figure.

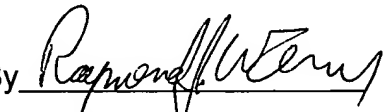
New Claims 10-11 are directed to a method of processing data, including generating digital data in a synchronous data processing unit; providing first digital data to an input of an asynchronous digital converting unit and holding the first digital data at the input; asynchronously computing a digital result in the asynchronous digital converting unit; and providing second digital data, subsequent to asynchronously computing the result, to the input of the asynchronous digital converting unit. Support for these Claims can be found in the specification from page 2, line 10, through page 4, line 9, and in the figure.

Conclusion

All of the objections and rejections in the outstanding Office Action of 13 April 2004 have been responded to, and Applicants respectfully submit that the pending Claims 1-11 are now in condition for allowance.

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

By 

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